DATA SHEET

OM6213
48 × 84 pixels matrix LCD driver

Product specification
File under Integrated Circuits, IC17

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Philips
Semiconductors

PHILIPS

CONTENTS

1 FEATURES

- Single-chip LCD controller/driver
- 48 row, 84 column outputs
- Display data RAM 48 × 84 bits
- On-chip:
  - Generation of LCD supply voltage (external supply also possible)
  - Generation of intermediate LCD bias voltages
  - Oscillator requires no external components (external clock also possible).
- External reset ($\overline{RES}$) input pin
- Serial interface maximum 4.0 Mbit/s
- CMOS compatible inputs
- Mux rate: 1 : 48
- Logic supply voltage range V_{DD1} to V_{SS}: 2.5 to 3.3 V
- Supply voltage range for high voltage part V_{DD2} to V_{SS}: 2.5 to 3.3 V
- Display supply voltage range V_{LCD} to V_{SS}: 4.5 to 9.0 V
- Low power consumption (typically 120 μA), suitable for battery operated systems
- Temperature compensation of V_{LCD}
- Temperature range: T_{amb} = −40 to +85 °C
- 5 Module Maker programmable parameters.

2 APPLICATIONS

- Telecommunications equipment.

3 GENERAL DESCRIPTION

The OM6213 is a low power CMOS LCD controller driver, designed to drive a graphic display of 48 rows and 84 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The OM6213 interfaces to microcontrollers via a serial bus interface.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM6213U	TRAY	chip with bumps in tray	–

5 BLOCK DIAGRAM

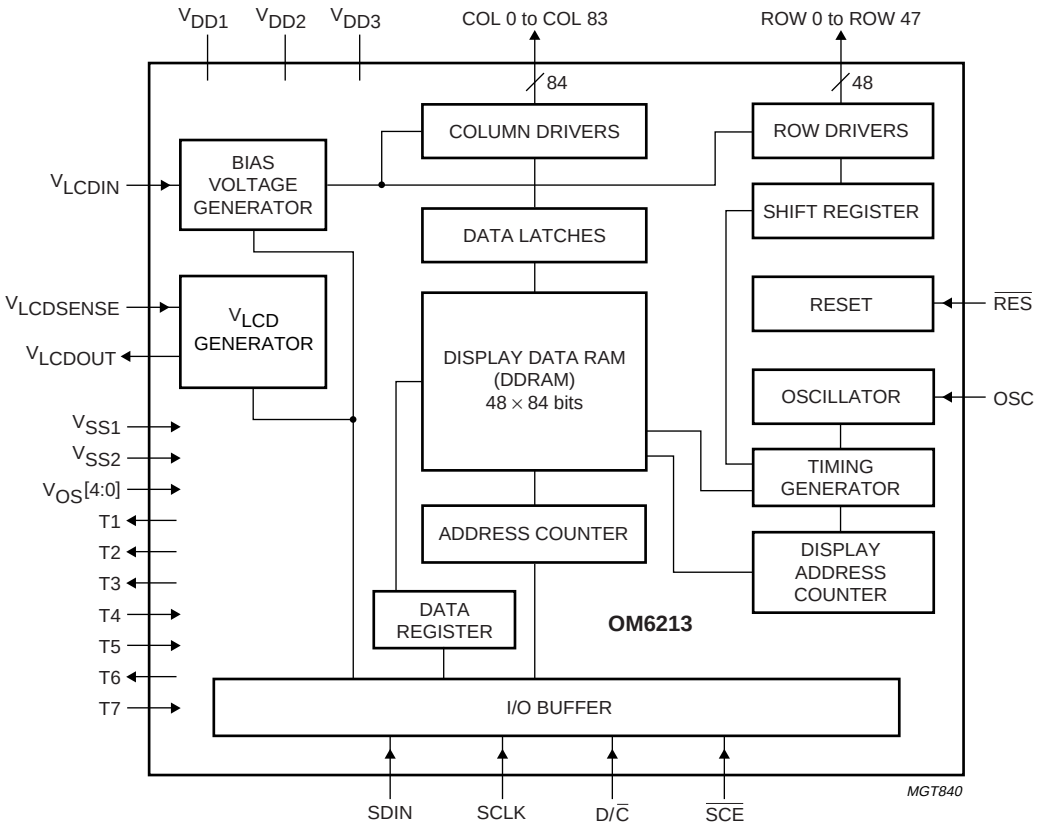


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD	DESCRIPTION
V_{OS4}	3	V_{LCD} offset pad 0 input
V_{OS3}	4	V_{LCD} offset pad 1 input
V_{OS2}	5	V_{LCD} offset pad 2 input
V_{OS1}	6	V_{LCD} offset pad 3 input
V_{OS0}	7	V_{LCD} offset pad 4 input
V_{DD1}	13 to 18	supply voltage 1
V_{DD3}	19 to 22	supply voltage 3
V_{DD2}	23 to 30	supply voltage 2
SCLK	31	serial clock input
T7	32 to 35	test 7 alternative HV-gen programming input
SDIN	36 to 39	serial data input and HV-gen programming input
D/$\overline{C}$	40	data/$\overline{\text{command}}$ input
$\overline{SCE}$	41	chip enable input (active LOW)
OSC	42	oscillator input
V_{SS2}	43 to 50	ground 2
T4	51	test 4 input
T5	52	test 5 input
T6	53	test 6 output
V_{SS1}	54 to 61	ground 1
T1	62	test 1 output
T2	63	test 2 output
T3	64	test 3 output
V_{LCDIN}	65 to 70	V_{LCD} supply voltage input and HV-gen programming input
V_{LCDOUT}	71 to 77	V_{LCD} generator output
$V_{LCDSENSE}$	78	V_{LCD} generator regulation input
$\overline{RES}$	79	reset input (active LOW)
ROW 11 to ROW 0	89 to 100	LCD row driver outputs
ROW 12 to ROW 23	101 to 112	LCD row driver outputs
COL 0 to COL 83	113 to 196	LCD column driver outputs
ROW 47 to ROW 36	197 to 208	LCD row driver outputs
ROW 24 to ROW 35	209 to 220	LCD row driver outputs
	1, 8 to 12, 81 to 88, 221 and 222	dummy pads

7 PIN FUNCTIONS

7.1 ROW 0 to ROW 47 row driver outputs

These pads output the row signals.

7.2 COL 0 to COL 83 column driver outputs

These pads output the column signals.

7.3 V_{SS1} and V_{SS2}: negative power supply rails

V_{SS1} and V_{SS2} must be connected together, jointly referred to as V_{SS}. When a pin has to be connected externally to V_{SS}, V_{SS1} should be used.

7.4 V_{DD1} to V_{DD3}: positive power supply rails

V_{DD1} provides the logic supply. V_{DD2} and V_{DD3} provide the analog supply; jointly referred to as V_{DD2}. V_{DD2} and V_{DD3} must be connected together.

7.5 V_{LCDOUT}, V_{LCDIN} and $V_{LCDSENSE}$: LCD power supplies

If the internal V_{LCD} generator is used, then all 3 pins must be connected together. If not (the internal V_{LCD} generator is disabled and an external voltage is supplied at pin V_{LCDIN}), V_{LCDOUT} must be left open-circuit and $V_{LCDSENSE}$ must be connected to V_{LCDIN}. V_{PR} must be set to logic 0 to switch-off the charge pump if an external V_{LCD} generator is used. V_{LCDIN} is also used for HV-gen programming.

7.6 V_{OS0} to V_{OS4}

Five input pins for on-glass V_{LCD} offset. Each pin must be connected to V_{SS1}, which corresponds to logic 0, or to V_{DD1}, which corresponds to logic 1. All five pins define a 5-bit two's complement number ranging from −16 to +15 decimal (from 10000 to 01111). The default value, with all pins connected to V_{SS1}, is 0 decimal (00000). The register is refreshed by each set bias system command or when exiting the Power-down mode.

7.7 T1 to T7: test pads

In the application, T4, T5 and T7 must be connected to V_{SS}. T1, T2, T3 and T6 must be left open-circuit.

7.8 SDIN: serial data line

Data line and HV-gen programming input.

7.9 SCLK: serial clock line

Input for the clock signal. 0 to 4.0 Mbits/s.

7.10 D/$\overline{C}$: mode select

Input to select either $\overline{\text{command}}$/address or data input.

7.11 $\overline{SCE}$: chip enable

The enable pin allows data to be clocked in; this signal is active LOW.

7.12 OSC: oscillator

If the on-chip oscillator is used, this input must be connected to V_{DD1}. If an external clock is used, it must be connected to pin OSC. If pin OSC is left at V_{SS1}, the internal clock is disabled, the device is not clocked and the display may be left in a DC state. To avoid this, it is advisable to enter the Power-down mode before stopping the clock.

7.13 $\overline{RES}$: reset

This signal will reset the device and must be applied to properly initialize the chip; this signal is active LOW.

8 BLOCK DIAGRAM FUNCTIONS

8.1 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required and the OSC input must be connected to V_{DD1}. If an external clock signal is used, it must be connected to pin OSC.

8.2 Address counter (AC)

The address counter assigns addresses to the display data RAM for writing. The X address X[6:0] and the Y address Y[2:0] are set separately. After a write operation the address counter is automatically incremented by 1 according to the V flag.

8.3 Display Data RAM (DDRAM)

The OM6213 contains a 48 × 84 bit static RAM which stores the display data. The RAM is divided into 6 banks of 84 bytes (6 × 8 × 84 bits). During RAM access, data is transferred to the RAM via the serial interface. There is a direct correspondence between the X address and the column output number.

8.4 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

8.5 Display address counter

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs.

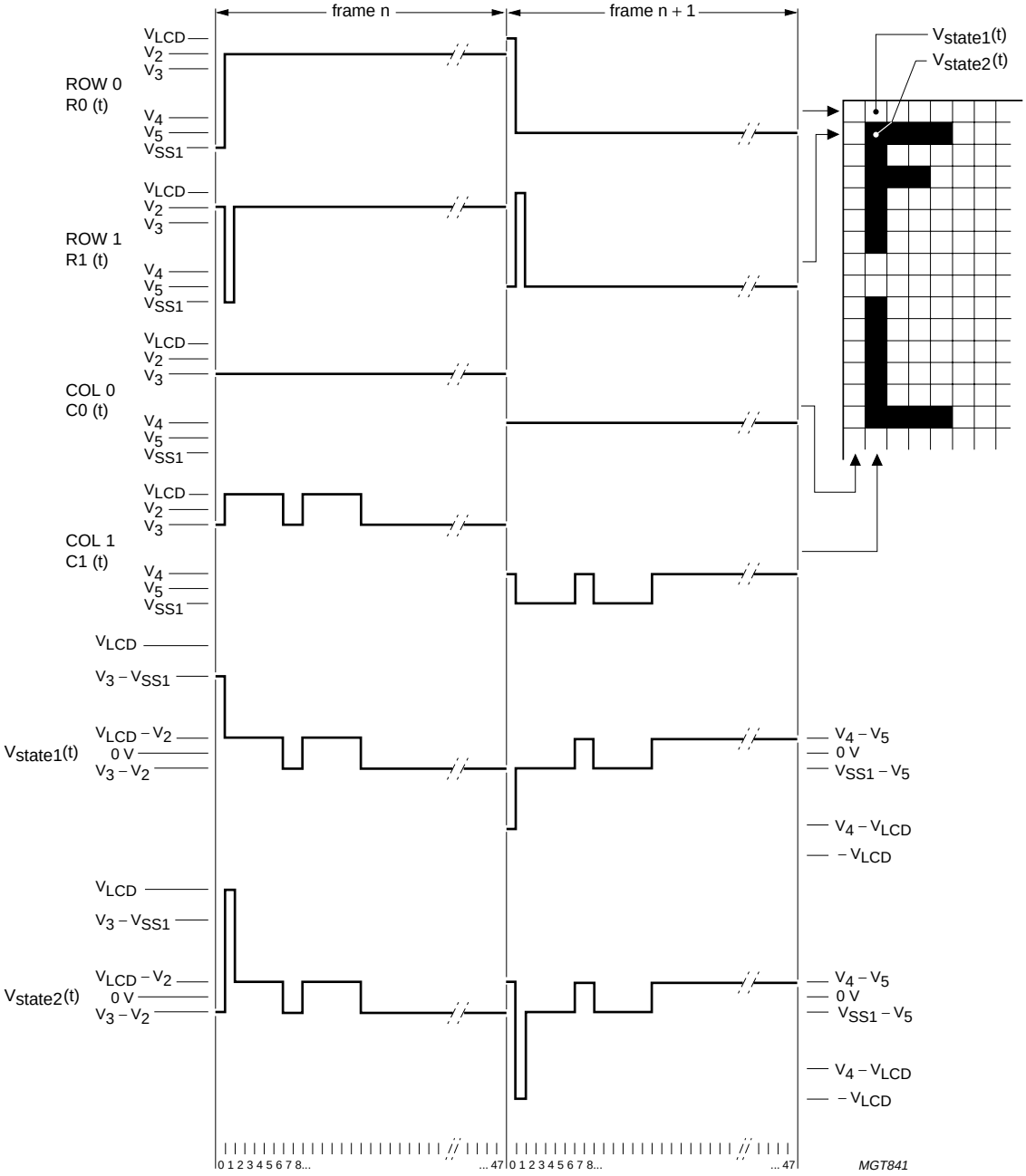
The display status (all dots on/off and normal/inverse video) is set by bits D and E in the command ‘Display control’ (see Table 2).

8.6 LCD row and column drivers

The OM6213 contains 48 rows and 84 column drivers, which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. Figure 2 shows typical waveforms. Unused outputs should be left unconnected.

8.7 V_{LCD} generator

The voltage multiplier (i.e. charge pump) generates the V_{LCD} voltage. The multiplication factor is Module Maker programmable (default value 4).



$V_{state1}(t) = C1(t) - R0(t)$
$V_{state2}(t) = C1(t) - R1(t)$

Fig.2 Typical LCD driver waveforms.

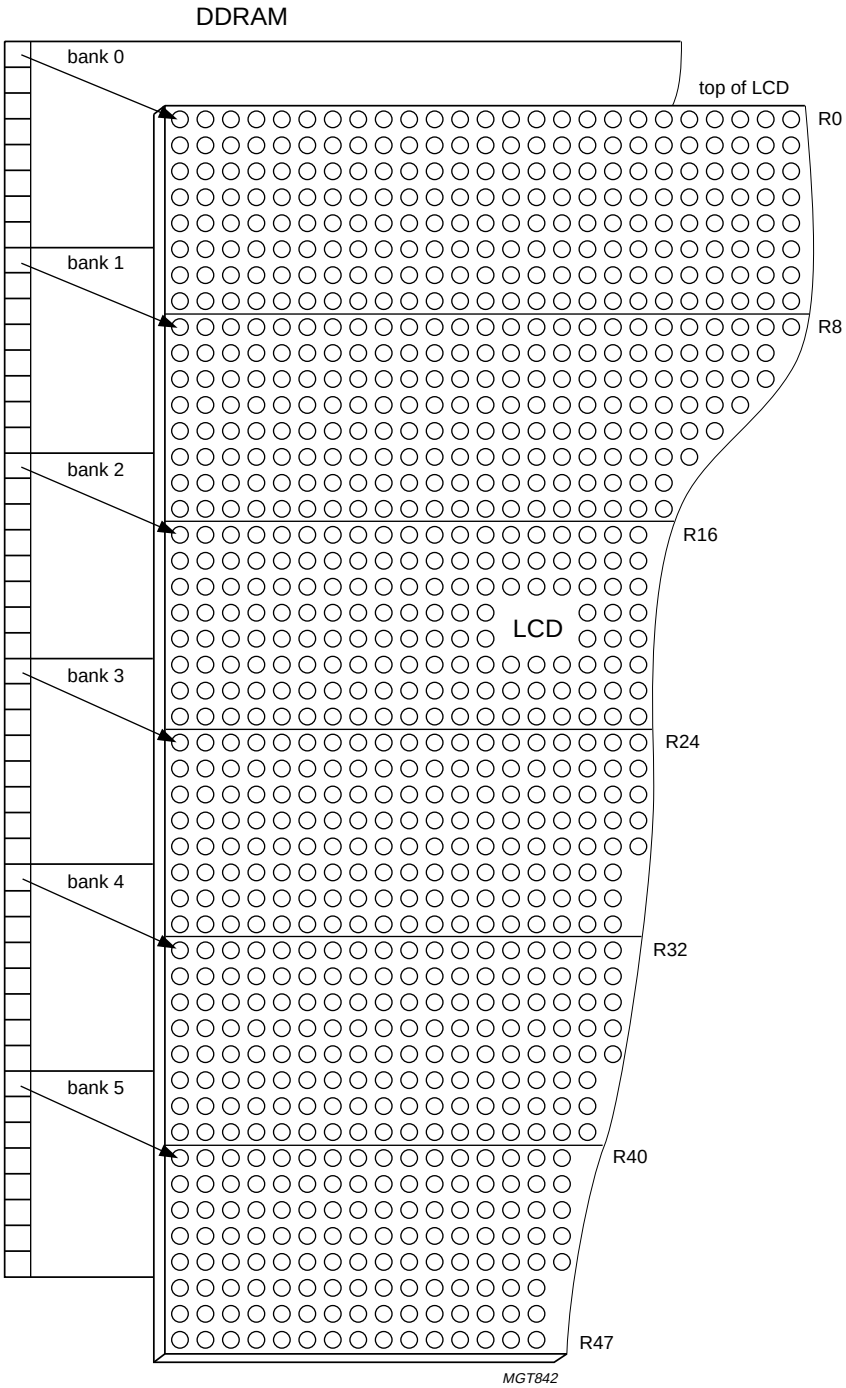


Fig.3 DDRAM to display mapping.

9 INITIALIZATION

Immediately following power-on, all internal registers and the RAM content are undefined. A reset ($\overline{RES}$) pulse must be applied. **It should be noted that the device may be damaged if not properly reset.**

Reset is accomplished by applying an external $\overline{RES}$ pulse (active LOW) at pad $\overline{RES}$. When reset occurs within the specified time, all internal registers are reset, however the RAM is still undefined. The state after reset is described in Section “Reset function”.

$\overline{RES}$ input must be $\leq 0.3V_{DD1}$ after V_{DD1} reaches $V_{DD(min)}$ (or higher) according to t_{VHRL} timing (see Fig.16)**.**

10 ADDRESSING

Data is downloaded in bytes into the RAM matrix of the OM6213 as indicated in Figs.3, 4, 5 and 6. The display RAM has a matrix of 48 × 84 bits. The columns are addressed by the address pointer.

The address ranges are: X = 0 to 83 (1010011) and Y = 0 to 5 (101). Addresses outside these ranges are not allowed.

In vertical addressing mode (V = 1) the Y address increments after each byte (see Fig.5). After the last Y address (Y = 5) Y wraps around to 0 and X increments to address the next column.

In horizontal addressing mode (V = 0) the X address increments after each byte; see Fig.6. After the last X address (X = 83) X wraps around to 0 and Y increments to address the next row.

After the very last address (X = 83 and Y = 5) the address pointers wrap around to address (X = 0 and Y = 0).

10.1 Data structure

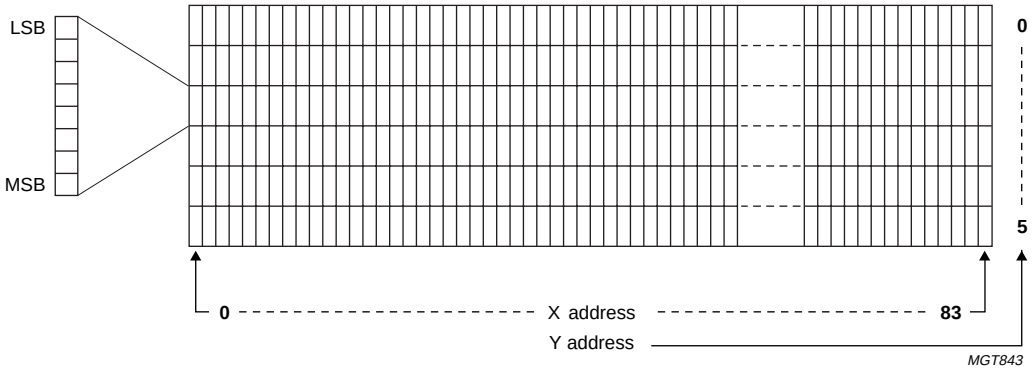


Fig.4 RAM format, addressing.

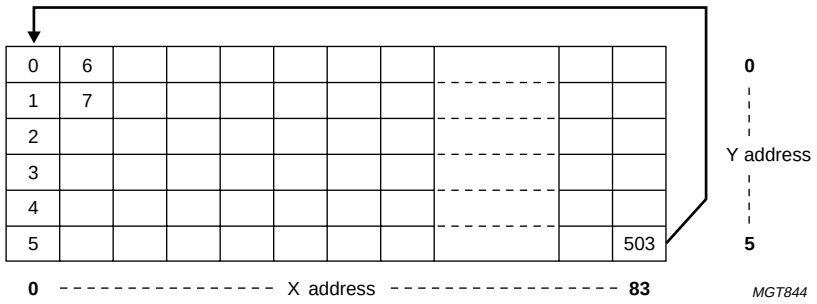


Fig.5 Sequence of writing data bytes into RAM with vertical addressing (V = 1).

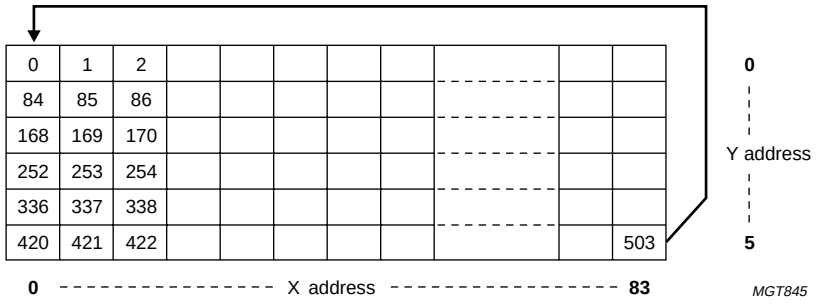


Fig.6 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

11 INSTRUCTIONS

The instruction format is divided into two modes. If D/$\overline{C}$ (mode select) is set LOW the current byte is interpreted as command byte (see Table 1). If D/$\overline{C}$ is set HIGH the following bytes are stored in the DDRAM. After every data byte the address counter is incremented automatically.

The level of the D/$\overline{C}$ signal is read during the last bit of the data byte.

Instructions can be sent in any order to the OM6213 (the exception being that the temperature control command must be followed by at least one byte of data or command). The MSB is transmitted first (see Fig.7). Figure 8 shows an example of a command stream, used to set-up the LCD driver.

The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state SCLK clock pulses have no effect and no power is consumed by the serial interface. A negative edge on $\overline{SCE}$ enables the serial interface and indicates the start of a data transmission.

Figures 9 and 10 show the serial bus protocol.

- When $\overline{SCE}$ is HIGH, SCLK clocks are ignored. During the HIGH time of $\overline{SCE}$ the serial interface is initialized (see Fig.11).
- SDIN is sampled at the positive edge of SCLK
- D/$\overline{C}$ indicates whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1). It is read with the eighth SCLK pulse.
- If $\overline{SCE}$ stays LOW after the last bit of a command/data byte, the serial interface expects bit DB7 of the next byte at the next rising edge of SCLK (see Fig.11)
- A reset pulse with $\overline{RES}$ interrupts the transmission. The data being written into the RAM may be corrupted. The registers are cleared. If $\overline{SCE}$ is LOW after the rising edge of $\overline{RES}$, the serial interface is ready to receive the D/$\overline{C}$ bit of a command/data byte (see Fig.12).
- Instructions (except the temperature control command) are executed on the SCLK positive edge which latches DB0 and D/$\overline{C}$
- The temperature control command is executed on the SCLK positive edge which latches DB0 and D/$\overline{C}$ of the next command or the next write to the DDRAM (whichever occurs first).This command requires 2 bytes to be executed.

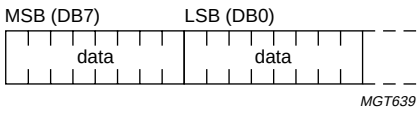


Fig.7 General format of data stream.

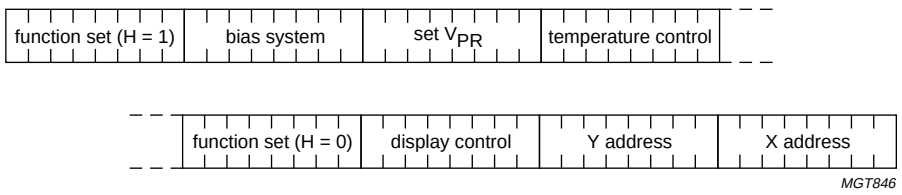


Fig.8 Serial data stream, example.

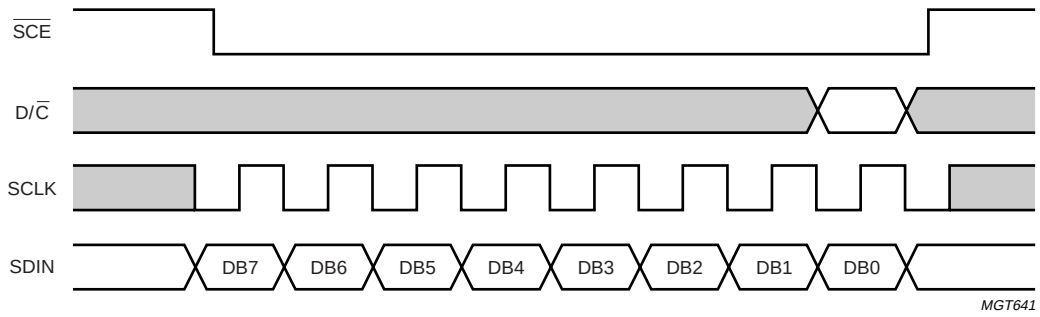


Fig.9 Serial bus protocol; transmission of one byte.

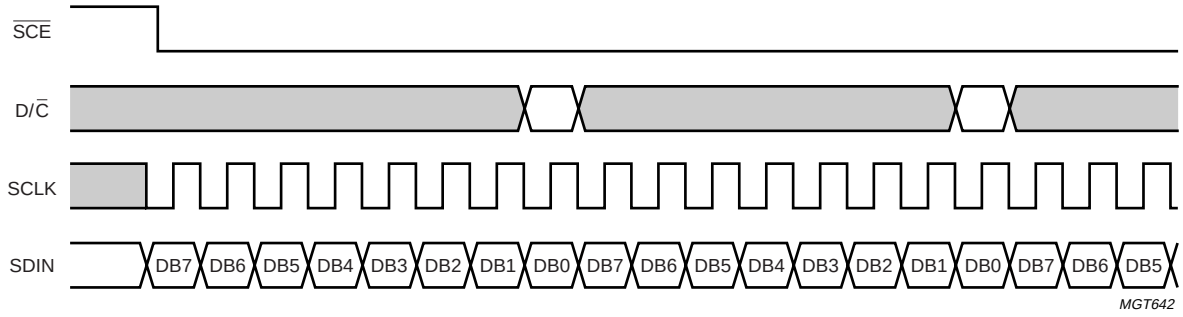


Fig.10 Serial bus protocol; transmission of several bytes.

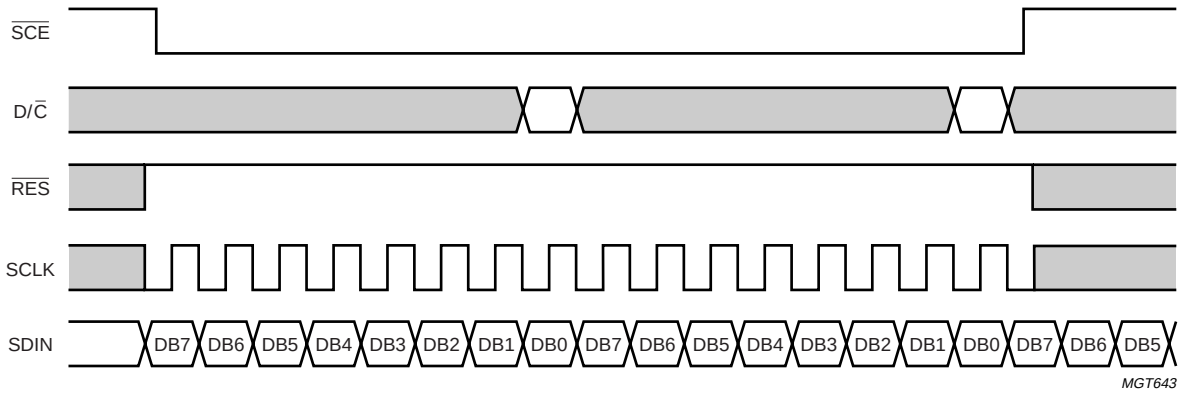


Fig.11 Serial bus reset function ($\overline{SCE}$).

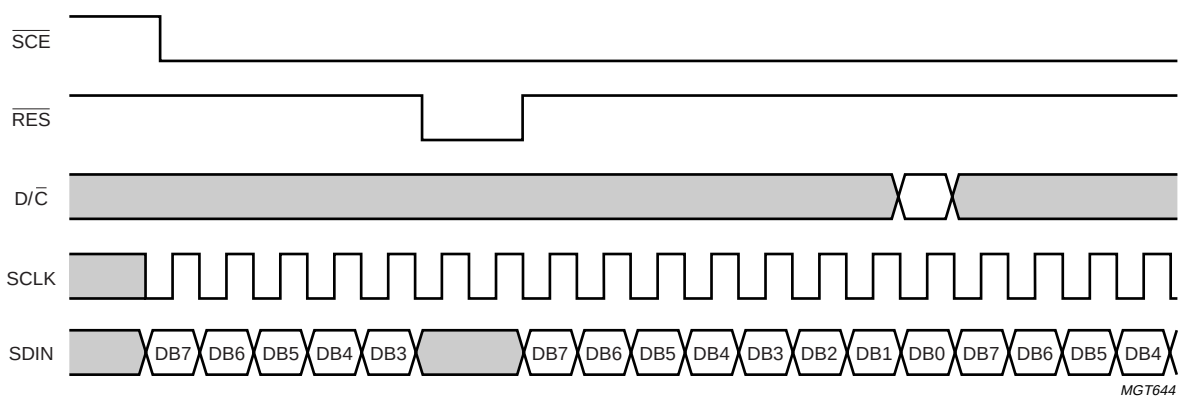


Fig.12 Serial bus reset function ($\overline{RES}$).

Table 1 Instruction set; see note 1 and Table 2

Instructions not expressly defined in Table 1 and reserved instructions must not be used in the application.

INSTRUCTION	D/$\overline{C}$	COMMAND BYTE								DESCRIPTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
(H = 0 or 1)										
NOP	0	0	0	0	0	0	0	0	0	no operation
Function set	0	0	0	1	0	0	PD	V	H	Power-down control; entry mode; extended instruction set control (H)
Write data	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	writes data to display RAM.
(H = 0)										
Reserved	0	0	0	0	0	0	0	1	X	reserved
Reserved	0	0	0	0	0	0	1	X	X	reserved
Display control	0	0	0	0	0	1	D	0	E	sets display configuration
Reserved	0	0	0	0	1	X	X	X	X	reserved
Set Y address of RAM	0	0	1	0	0	0	Y_2	Y_1	Y_0	sets Y address of RAM; $0 \leq Y \leq 5$
Set X address of RAM.	0	1	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Sets X address part of RAM; $0 \leq Y \leq 5$
(H = 1)										
Reserved	0	0	0	0	0	0	0	1	X	reserved
Temperature control	0	0	0	0	0	0	1	TC_1	TC_0	set temperature coefficient (TCx)
Reserved	0	0	0	0	0	1	X	X	X	reserved
Bias system	0	0	0	0	1	0	BS_2	BS_1	BS_0	set bias system (BSx)
Reserved	0	0	1	X	X	X	X	X	X	reserved
Set V_{PR}	0	1	V_{PR6}	V_{PR5}	V_{PR4}	V_{PR3}	V_{PR2}	V_{PR1}	V_{PR0}	write V_{PR} to register

Note

1. X = don’t care.

Table 2 Explanations for symbols in Table 1

BIT		LOGIC 0	LOGIC 1
PD		chip is active	chip is in Power-down mode
V		horizontal addressing	vertical addressing
H		use basic instruction set	use extended instruction set
D, E	00	display blank	
	10	normal mode	
	01	all display segments on	
	11	inverse video mode	
TC1 and TC0	00 (TC0)	V_{LCD} temperature coefficient TCA	
	01 (TC1)	Module Maker defined; V_{LCD} temperature coefficient	
	10 (TC2)	V_{LCD} temperature coefficient TCC	
	11 (TC3)	V_{LCD} temperature coefficient TCD	

11.1 Reset function

After reset the LCD driver has the following state:

- Power-down mode (PD = 1)
- Horizontal addressing (V = 0) normal instruction set (H = 0)
- Display blank (E = D = 0)
- Address counter X[6:0] = 0, Y[2:0] = 0
- Temperature control mode (TC[1:0] = 0, TC0, TCA)
- Bias system (BS[2:0] = 0)
- V_{LCD} is equal to 0, the HV-generator is switched off (V_{PR}[6:0] = 0)
- After power-on, RAM data is undefined
- Oscillator off (external clock operation is possible).

11.2 Function set

11.2.1 PD

- All LCD outputs at V_{SS1} (display off)
- Bias generator and V_{LCD} generator off, V_{LCD} can be disconnected
- Oscillator off
- Serial bus, command, etc. function
- RAM contents not cleared; RAM data can be written.

11.2.2 V

When V = 0, horizontal addressing is selected. The data is written into the DDRAM as shown in Fig.6. When V = 1, vertical addressing is selected. The data is written into the DDRAM as shown in Fig.5.

11.2.3 H

When H = 0 the commands ‘display control’, ‘set Y address’ and ‘set X address’ can be performed, when H = 1 the others can be executed. The commands ‘write data’ and ‘function set’ can be executed in both cases.

11.3 Display Control

11.3.1 D, E

The bits D and E select the display mode (see Table 2).

11.4 Set Y address of RAM

Y2 to Y0 defines the Y address vector address of the display RAM; see Table 3.

Table 3 Y address range

Y2	Y1	Y0	CONTENT
0	0	0	bank 0
0	0	1	bank 1
0	1	0	bank 2
0	1	1	bank 3
1	0	0	bank 4
1	0	1	bank 5

11.5 Set X address of RAM

The X address points to the columns. The range of X is 0 to 83 (53H).

11.6 Temperature Control

The temperature coefficient of V_{LCD} is selected by the two bits TC1 and TC0.

11.7 Bias value

The bias voltage levels are set in the ratio of R - R - nR - R - R giving a $\frac{1}{(n+4)}$ bias system. Different multiplex rates require different factors of 'n' (see Table 4). This is programmed by BS[2:0]. For Mux 1 : 48 the optimum bias value 'n' is given by $n = \sqrt{48} - 3 = 3.928 = 4$ resulting in $1/8$ bias.

Table 4 Programming the required bias system

BS2	BS1	BS0	n	BIAS SYSTEM	RECOMMENDED MUX RATE
0	0	0	7	$1/11$	1 : 100
0	0	1	6	$1/10$	1 : 80
0	1	0	5	$1/9$	1 : 65
0	1	1	4	$1/8$	1 : 48
1	0	0	–	Module Maker programmable (see Table 11)	–
1	0	1	2	$1/6$	1 : 24
1	1	0	1	$1/5$	1 : 18/1 : 16
1	1	1	0	$1/4$	1 : 10/1 : 9/1 : 8

Table 5 LCD bias voltage

SYMBOL	BIAS VOLTAGE FOR $1/8$ BIAS SYSTEM
V1	V_{LCD}
V2	$7/8 \times V_{LCD}$
V3	$6/8 \times V_{LCD}$
V4	$2/8 \times V_{LCD}$
V5	$1/8 \times V_{LCD}$
V6	V_{SS}

11.8 V_{LCD} generator

The binary number V_{OP} representing the operating voltage can be set by the serial interface command and can be adjusted (calibrated) by 5 input pins according to the following formulae:

$$V_{OP} = V_{OS} + V_{CAL} + (2 \times V_{PR}) \quad (1)$$

where:

- V_{OP} is an 8-bit unsigned number used internally for generation of the LCD supply voltage V_{LCD}
- V_{OS} is a 5-bit two's complement number set by the 5 input pins V_{OS}[4:0]; see Table 6
- V_{CAL} is a 5-bit two's complement number set by the Module Maker; see Table 7
- V_{PR} is a 7-bit unsigned number set by the serial interface command.

To avoid numerical overflow the allowed values of V_{PR} should be limited to the range $V_{PR(min)}$ to $V_{PR(max)}$ (decimal).

The corresponding voltage at the reference temperature, T_{CUT}, can be calculated as:

$$V_{LCD(Tcut)} = (a + V_{OP} \times b) \quad (2)$$

The generated voltage at V_{LCD} is dependent on the temperature, programmed temperature coefficient (TC) and the programmed voltage at the reference temperature (T_{CUT}).

$$V_{LCD} = (a + V_{OP} \times b) \times [1 + TC \times (T - T_{CUT})] \quad (3)$$

T_{CUT}, a and b for each temperature coefficient are given in Table 6. The maximum voltage that can be generated is dependent on the voltage of V_{DD2} and the display load current.

As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD}, the user has to ensure while setting the V_{PR} register and selecting the Temperature Compensation (TC), that under all conditions and including all tolerances the V_{LCD} limit of maximum 9 V will never be exceeded.

For a particular liquid, the optimum V_{LCD} can be calculated for a given multiplex rate. For a mux rate of 1 : 48, the optimum operating voltage of the liquid can be calculated as follows;

$$V_{LCD} = \frac{1 + \sqrt{48}}{\sqrt{2 \cdot \left(1 - \frac{1}{\sqrt{48}}\right)}} \cdot V_{th} = 6.06 \cdot V_{th} \quad (4)$$

where V_{th} is the threshold voltage of the liquid crystal used.

Table 6 Typical values for parameters of the HV generator programming

SYMBOL	TCA	TCB	TCC	TCD	UNIT
a	3.06	3.84	3.62	3.37	V
b	30.3	24.3	26.1	28.0	mV
T_{CUT}	27	27	27	27	°C
TC	0	–0.87	–0.58	–0.29	10^{-3}/°C
$V_{PR(min)}$	49	20	30	39	decimal
$V_{PR(max)}$	127	101	110	120	decimal
$V_{LCD(min)}$	6.04	4.81	5.18	5.56	V
$V_{LCD(max)}$	10.77	8.74	9.35	10.11	V

$V_{LCD(min)}$ values are the values corresponding to $V_{PR(min)}$.

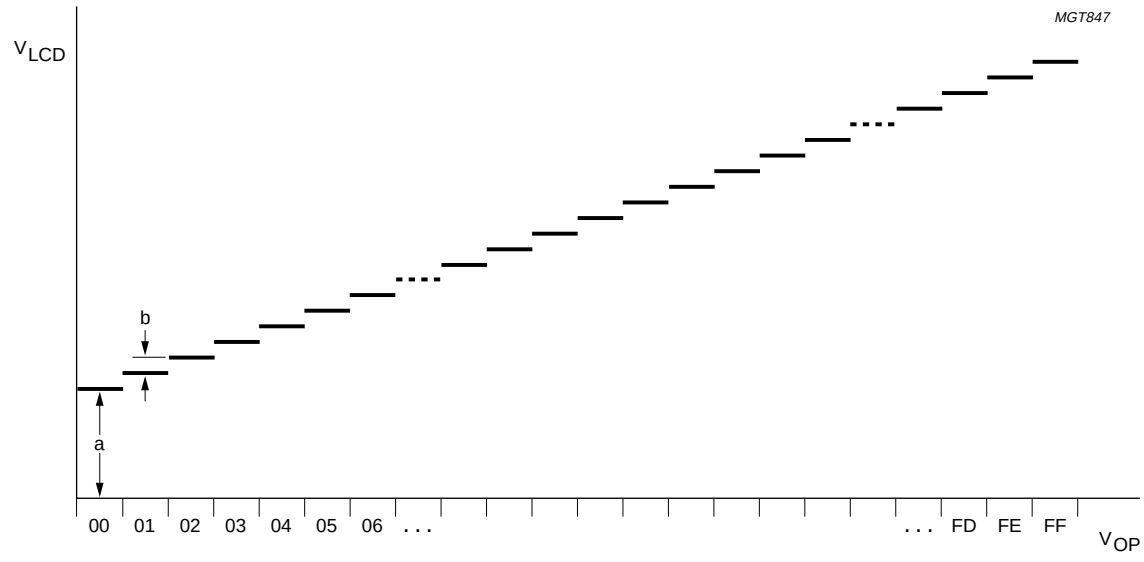
$V_{LCD(max)}$ values are the theoretical values corresponding to $V_{PR(max)}$. Under all conditions and including all tolerances V_{LCD} must never exceed 9 V.

Example: V_{PR} is set to 63 (decimal) and TCB is selected. At temperature T_{CUT} the measured V_{LCD} is 6.9 V. The user wants to decrease V_{LCD} by 100 mV in order to set V_{LCD} to 6.8 V. The best value for V_{OS} is then –4 decimal (11100 binary in the two's complement notation).

If V_{PR}[6:0] is set to zero, the charge pump is turned off.

Table 7 V_{OS} and V_{CAL} values in two's complement notation

DECIMAL	BINARY
0	00000
1	00001
2	00010
3	00011
4	00100
5	00101
6	00110
7	00111
8	01000
9	01001
10	01010
11	01011
12	01100
13	01101
14	01110
15	01111
–1	11111
–2	11110
–3	11101
–4	11100
–5	11011
–6	11010
–7	11001
–8	11000
–9	10111
–10	10110
–11	10101
–12	10100
–13	10011
–14	10010
–15	10001
–16	10000



V_{OP} 7 to 0 programming (00H to FFH).
Depending on V_{PR} restrictions defined in Table 6 and depending on V_{OS} and V_{CAL}, not all V_{OP}[7:0] can be selected.
If V_{PR} is set to 0, the charge pump is turned off and V_{LCD} = 0 V if no external V_{LCD} supply is provided.

Fig.13 V_{LCD} programming of the OM6213.

12 TEMPERATURE COMPENSATION

Due to the temperature dependency of the liquid crystal viscosity, the LCD controlling voltage V_{LCD} must be increased with lower temperature to maintain optimum contrast. Figure 14. shows V_{LCD} for high multiplex rates. In the OM6213 the temperature coefficient of V_{LCD} can be selected from 4 values (see Table 2) by setting bits TC[1:0].

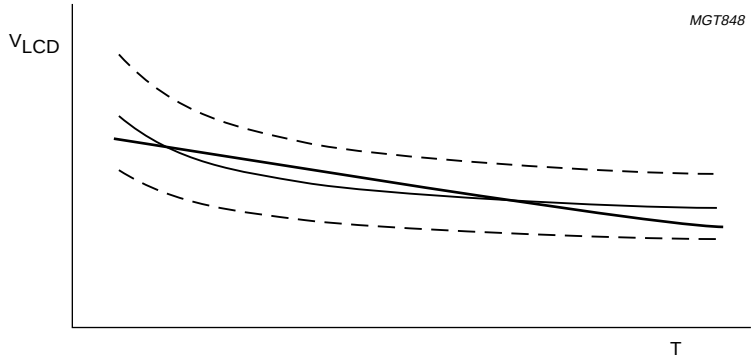


Fig.14 V_{LCD} as a function of liquid crystal temperature (typical values).

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); see notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	logic supply voltage	–0.5	+6.5	V
$V_{DD2,3}$	high supply voltage	–0.5	+6.5	V
V_{LCD}	LCD supply voltage	–0.5	+10	V
V_i	all input voltages	–0.5	V_{DD1} + 0.5	V
I_{SS}	ground supply current	–50	+50	mA
I_I, I_o	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	100	mW
P_{out}	power dissipation per output	–	10	mW
T_{amb}	ambient temperature	–40	+85	℃
T_{jun}	junction temperature	–65	+150	°C
T_{stg}	storage temperature	–65	+150	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are referenced to V_{SS1} unless otherwise noted.

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *“Handling MOS devices”*).

15 DC CHARACTERISTICS

V_{DD1} = V_{DD2} = 2.5 to 3.3 V; V_{SS} = 0 V; V_{LCD} = 4.5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	logic supply voltage		2.5	–	3.3	V
$V_{DD2,3}$	high supply voltage		2.5	–	3.3	V
V_{LCD}	LCD supply voltage	note 1	4.5	–	9.0	V
I_{DD1}	total (V_{DD1} + V_{DD2} + V_{DD3}) supply current 1	normal mode; V_{DD1} = V_{DD2} = V_{DD3} = 2.85 V; V_{LCD} = 6.9 V (4 booster device); f_{SCLK} = 0; T_{amb} = 25 °C; display load = 10µA; inputs at V_{DD1} or V_{SS}, bias system 1/7; note 2	–	120	–	µA
I_{DD2}	supply current 2	Power-down mode; with internal or external LCD supply voltage; inputs at V_{DD1} or V_{SS}; note 3	–	3	–	µA
I_{DD3}	supply current external V_{LCD}	V_{DD1} = V_{DD2} = V_{DD3} = 2.85 V; V_{LCD} = 6.9 V; f_{SCLK} = 0; T_{amb} = 25 °C; display load = 10 µA; inputs at V_{DD1} or V_{SS}; bias system 1/7; notes 2 and 5	–	20	–	µA
I_{LCDIN}	supply current from external V_{LCD}	V_{DD1} = V_{DD2} = V_{DD3} = 2.85 V; V_{LCD} = 6.9 V; f_{SCLK} = 0; T_{amb} = 25 °C; display load = 10 µA; inputs at V_{DD1} or V_{SS}; bias system 1/7; notes 2, 4 and 5	–	25	–	µA
Logic						
V_{IL}	LOW-level input voltage		V_{SS}	–	0.3V_{DD1}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD1}	–	V_{DD1}	V
I_{LI}	input leakage current	V_i = V_{DD1} or V_{SS}	–1	–	+1	µA
Column and row outputs						
$R_{o(col)}$	column output resistance COL0 to COL83	note 6	–	4	20	kΩ
$R_{o(row)}$	row output resistance ROW0 to ROW47	note 6	–	4	20	kΩ
$V_{bias(col)}$	bias tolerance COL0 to COL83		–100	0	+100	mV
$V_{bias(row)}$	bias tolerance ROW0 to ROW47		–100	0	+100	mV
LCD supply voltage generator						
$V_{LCD(tol)}$	V_{LCD} tolerance internally generated	note 7	–70	–	+70	mV

Notes to the DC characteristics

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Internal clock.
3. Power-down mode: during Power-down all static currents are switched off.
4. If external V_{LCD}, the display load current is not transmitted to I_{DD}.
5. V_{LCD} external voltage applied to V_{LCDIN} and $V_{LCDSENSE}$ inputs; V_{LCDOUT} disconnected. V_{PR} must be set to 0 to switch-off the charge pump.
6. Load current 10 μA, outputs tested one at a time.
7. Valid for values of temperature, V_{OP} and TC used at the calibration.

16 AC CHARACTERISTICS

$V_{DD1} = V_{DD2} = 2.5$ V to 3.3 V; $V_{SS} = 0$ V; $V_{LCD} = 4.5$ to 9.0 V; $T_{amb} = -40$ to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_{clk(ext)}$	external clock frequency		30.9	34.3	37.7	kHz
f_{frame}	frame frequency	internal oscillator; note 1	63	70	77	Hz
t_{VHRL}	reset LOW pulse set-up time after power-on	notes 2 and 3; see Fig.16	0	–	30	μs
t_{RW}	reset LOW pulse width	see Fig.16	100	–	–	ns
$t_{R(op)}$	end of reset pulse to interface being operational		–	–	1000	ns
Serial bus timing characteristics						
f_{SCLK}	clock frequency	V_{DD1} = 3.0 V ±10%; all signal timing is based on 20% to 80% of V_{DD} and a maximum rise and fall time of 10 ns	0	–	4.00	MHz
$T_{cy(SCLK)}$	clock cycle time SCLK		250	–	–	ns
t_{PWH1}	SCLK pulse width HIGH		100	–	–	ns
t_{PWL1}	SCLK pulse width LOW		100	–	–	ns
t_{S2}	$\overline{SCE}$ set-up time		60	–	–	ns
t_{H2}	$\overline{SCE}$ hold time		100	–	–	ns
t_{PWH2}	$\overline{SCE}$ minimum HIGH time		100	–	–	ns
t_{H5}	$\overline{SCE}$ start hold time	note 4	100	–	–	ns
t_{S3}	D/$\overline{C}$ set-up time		100	–	–	ns
t_{H3}	D/$\overline{C}$ hold time		100	–	–	ns
t_{S4}	SDIN set-up time		100	–	–	ns
t_{H4}	SDIN hold time		100	–	–	ns

Notes

1. $t_{frame} = f_{clk(ext)}/490$.
2. $\overline{RES}$ may be LOW before V_{DD} goes HIGH (see Fig.16). This is recommended.
3. Decoupling capacitor V_{LCD}/V_{SS1} = 100 nF (higher capacitor size increases t_{VHRL} or higher $V_{DD1,2,3}$ reduces t_{VHRL}).
4. t_{H5} is the time from the previous SCLK positive edge (irrespective of the state of $\overline{SCE}$) to the negative edge of $\overline{SCE}$ (see Fig.15).

17 SERIAL INTERFACE

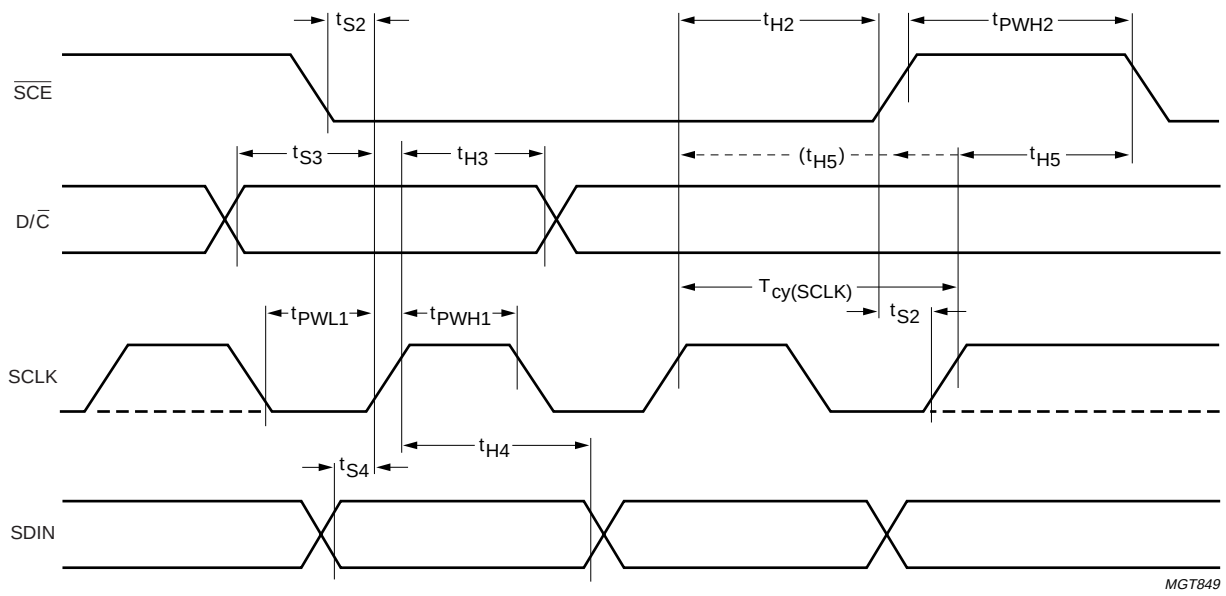


Fig.15 Serial interface timing.

18 RESET

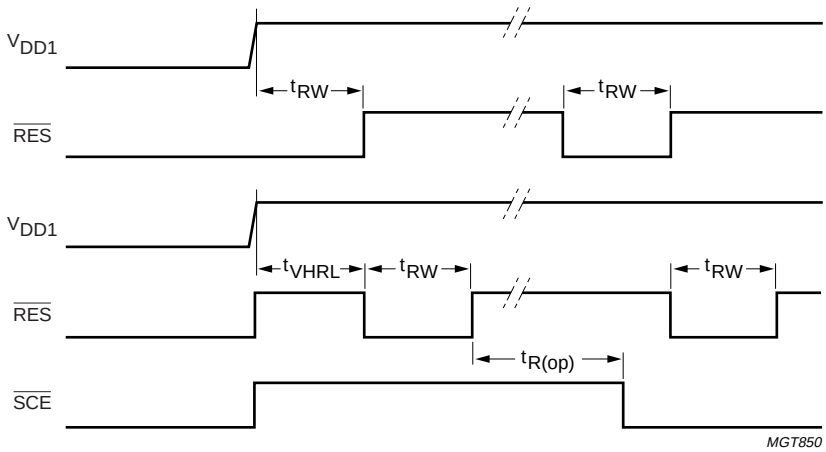
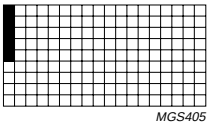
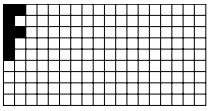
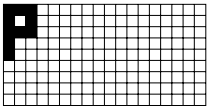
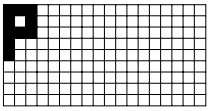
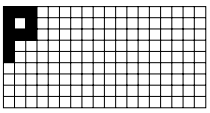
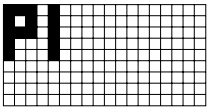
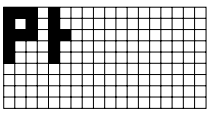


Fig.16 Reset timing.

19 APPLICATION INFORMATION

Table 8 Example of OM6213 operation

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1	Start										$\overline{SCE}$ is going LOW
2	0	0	0	1	0	0	0	0	1		function set; PD = 0, V = 0, select extended instruction set (H = 1 mode)
3	0	1	0	0	1	0	0	0	0		set V_{PR}; V_{PR} is set to 16
4	0	0	0	1	0	0	0	0	0		function set; PD = 0, V = 0, select normal instruction set (H = 0 mode)
5	0	0	0	0	0	1	1	0	0		display control; set normal mode (D = 1, E = 0)
6	1	0	0	0	1	1	1	1	1	 MGS405	data write; Y and X are initialized to 0 by default, so they are not set here
7	1	0	0	0	0	0	1	0	1	 MGS406	data write
8	1	0	0	0	0	0	1	1	1	 MGS407	data write
9	1	0	0	0	0	0	0	0	0	 MGS407	data write
10	1	0	0	0	1	1	1	1	1	 MGS408	data write
11	1	0	0	0	0	0	1	0	0	 MGS409	data write
12	1	0	0	0	1	1	1	1	1	 MGS410	data write

STEP	SERIAL BUS BYTE									DISPLAY	OPERATION
	D/$\overline{C}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
13	0	0	0	0	0	1	1	0	1	 MGS412	display control; set inverse video mode (D = 1, E = 1)
14	0	1	0	0	0	0	0	0	0	 MGS412	set X address of RAM; set address to 0000000
15	1	0	0	0	0	0	0	0	0	 MGS414	data write

The pinning of the OM6213 is optimized for single plane wiring e.g. for chip-on-glass display modules. Display size: 48 × 84 pixels.

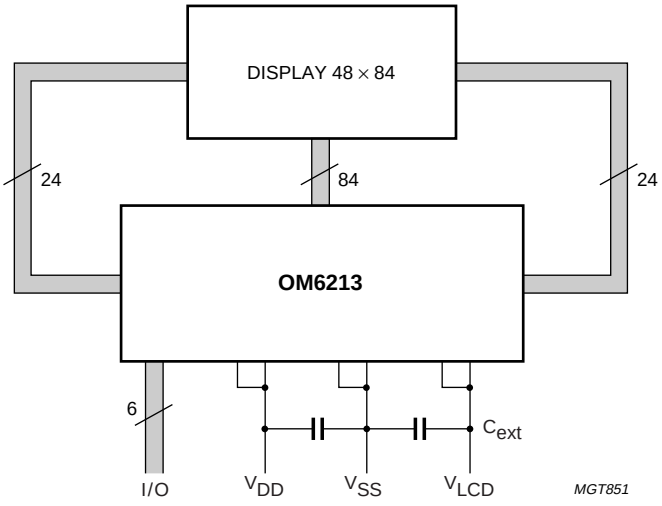


Fig.17 Application diagram.

The required minimum value for the external capacitors in an application with the OM6213 are:

C_{ext} = 100 nF (min.) for $V_{LCD1,2}/V_{SS1,2}$, C_{ext} = 1.0 µF (min.) for $V_{LCD1,2,3}/V_{SS1,2}$

Higher capacitor values are recommended for ripple reduction.

20 Module Maker programming

The OM6213 features five Module Maker programmable parameters:

1. V_{LCD} calibration
2. Charge pump multiplication factor
3. Bias system selected when BS[2:0] = 100
4. V_{LCD} temperature coefficient selected when TC[1:0] = 01 (TC1)
5. Seal bit. Used to select the use of the default parameters or the Module Maker programmable parameters. Once set:
   a) **The seal bit cannot be reset**
   b) The Module Maker programmable parameters cannot be changed
   c) The Module Maker programmable parameters are selected and the default parameters are deselected.

20.1 V_{LCD} calibration

The first parameter calibrates the V_{LCD} voltage.

A 5-bit code (V_{CAL}[4:0]) is used for this parameter. The code is implemented in two's complement notation giving rise to a positive or negative offset to the V_{PR} register. V_{LCD} calibration may be used together with V_{LCD} offset (performed by connecting the V_{OS}[4:0] pads to either V_{SS1} or to V_{DD1}).

V_{PR} values must always be within the ranges specified in Table 6.

$$V_{OP} = V_{OS} + V_{CAL} + (2 \times V_{PR}) \quad (5)$$

$$V_{LCD} = a + V_{OP} \times b \text{ at } T_{nom} \quad (6)$$

V_{LCD} can be calculated from equations (5) and (6): a and b are parameters defined in Table 6. An example of the correspondence between the V_{CAL} code and the relative V_{LCD} calibration is shown in Table 9, where b is assumed to be 24.3 mV (TCB, temperature coefficient B) and V_{OS} is assumed to be 0.

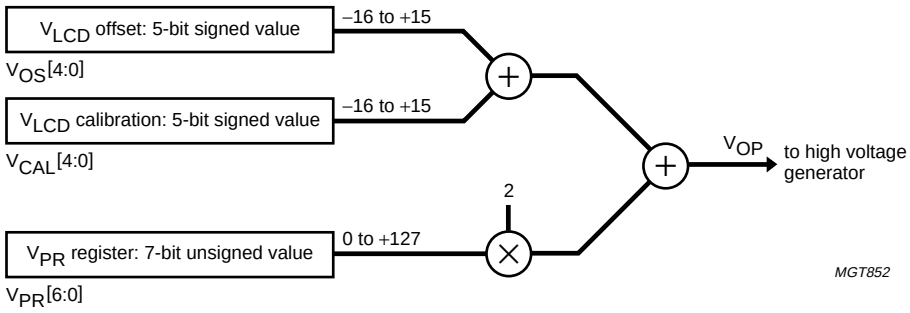


Fig.18 V_{LCD} offset and calibration

Table 9 V_{CAL} codes and associated nominal calibration voltage (TCB, V_{OS} = 0)

V_{CAL}[4:0]	V_{CAL}	V_{LCD} CALIBRATION (mV) (TCB, V_{OS} = 0)
00000	0	0 mV (default)
00001	1	+24.3
00010	2	+48.6
00011	3	+72.9
00100	4	+97.2
00101	5	+121.5
00110	6	+145.8
00111	7	+170.1
01000	8	+194.4
01001	9	+218.7
01010	10	+243
01011	11	+267.3
01100	12	+291.6
01101	13	+315.9
01110	14	+340.2
01111	15	+364.5
11111	–1	–24.3
11110	–2	–48.6
11101	–3	–72.9
11100	–4	–97.2
11011	–5	–121.5
11010	–6	–145.8
11001	–7	–170.1
11000	–8	–194.4
10111	–9	–218.7
10110	–10	–243
10101	–11	–267.3
10100	–12	–291.6
10011	–13	–315.9
10010	–14	–340.2
10001	–15	–364.5
10000	–16	–388.8

20.2 Charge pump multiplication factor

The second parameter defines the charge pump multiplication factor.

A 1-bit code (MF) is used for this parameter.

Table 10 Charge pump multiplication factor definition

MF	MULTIPLICATION FACTOR
0	4 (default)
1	3

20.3 Bias system selected when BS[2:0] = 100

The third parameter defines the bias system selected when BS[2:0] = 100.

A 1-bit code (BS100) is used for this parameter.

Table 11 Bias system selected when BS[2:0] = 100 definition

BS 00	BIAS SYSTEM
0	1⁄7 (default)
1	1⁄6

20.4 V_{LCD} temperature coefficient selected when TC[1:0] = 01 (TC1)

The fourth parameter defines the V_{LCD} temperature coefficient selected when TC[1:0] = 01 (TC1).

TC1 may be defined by using a two bit code (TCx[1:0]).

Table 12 V_{LCD} temperature coefficient

TC[1:0]	TC1[1:0]	V_{LCD} TEMPERATURE COEFFICIENT
00 (TC0)		TCA
01 (TC1)	00	TCB (default)
	01	TCA
	10	TCD
	11	TCC
10 (TC2)		TCC
11 (TC3)		TCD

20.5 Seal bit

The seal bit selects between the default parameters and the Module Maker programmed parameters. The seal bit prevents further changes to the Module Maker programmable parameters. A 1-bit code (SB) is used for this parameter. The seal bit, once set to 1, cannot be reset to 0.

Table 13 Seal bit definition

SB	PARAMETERS	MODULE MAKER PROGRAMMABLE PARAMETERS
0	defaults	programming possible
1	Module Maker programmable	programming prevented

20.6 Module Maker parameter programming

Module Maker programmable parameters are stored in 10 non-volatile cells.

Table 14 Non-volatile cell list

CELL[9:0]	DESCRIPTION
9	$V_{CAL}[4]$
8	$V_{CAL}[3]$
7	$V_{CAL}[2]$
6	$V_{CAL}[1]$
5	$V_{CAL}[0]$
4	MF
3	BS100
2	TC1[1]
1	TC1[0]
0	SB

An unprogrammed cell contains 0. A programmed cell contains 1. OM6213 dice are shipped to the Module Maker with all cells unprogrammed (containing 0). An unprogrammed cell may be programmed by using the described procedure. A programmed cell cannot be unprogrammed to 0.

Table 15 Module Maker parameters programming procedure

STEP	D/$\overline{C}$	COMMAND BYTE								ACTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1										switch power on
2										reset the device ($\overline{RES}$ pulse)
3	0	0	0	0	1	0	0	0	0	exit Power-down and set H = 0 instruction set
4										wait 5 ms
5	0	0	0	0	1	0	0	1	0	enter Power-down
6	0	0	0	0	0	0	0	1	0	enter programming mode
7	0	1	0	0	0	0	0	0	CELL[9]	specify CELL[9] (V_{CAL}[4])
8	0	1	0	0	0	0	0	0	CELL[8]	specify CELL[8] (V_{CAL}[3])
9	0	1	0	0	0	0	0	0	CELL[7]	specify CELL[7] (V_{CAL}[2])
10	0	1	0	0	0	0	0	0	CELL[6]	specify CELL[6] (V_{CAL}[1])
11	0	1	0	0	0	0	0	0	CELL[5]	specify CELL[5] (V_{CAL}[0])
12	0	1	0	0	0	0	0	0	CELL[4]	specify CELL[4] (MF)
13	0	1	0	0	0	0	0	0	CELL[3]	specify CELL[3] (BS100)
14	0	1	0	0	0	0	0	0	CELL[2]	specify CELL[2] (TC1[1])
15	0	1	0	0	0	0	0	0	CELL[1]	specify CELL[1] (TC1[0])
16	0	1	0	0	0	0	0	0	CELL[0]	specify CELL[0] (SB)
17										apply programming waveforms
18										go back to step 7 if other cells need to be programmed (see note 5)
19	0	0	0	0	0	0	0	0	0	exit programming mode
20										switch power off

Notes

1. Programming voltages are applied via pins SDIN and VLCDIN.
2. It is possible to program only one cell at a time. When applying programming waveforms, all cells (except the one being programmed) should be 0; see also example in note 5.
3. The seal bit (SB) must be the last to be programmed, since no further programming is possible when SB = 1.
4. If the seal bit is unprogrammed (SB = 0) the defaults (and not the Module Maker programmed parameters) are taken into account.
5. Example: a device has to be programmed to use a charge pump with a multiplication factor equal to 3 (initial state is MF = SB = 0, final state is MF = SB = 1).
   a) Execute steps 1 to 6.
   b) Set CELL[9:0] to 0000010000 (steps 7 to 16).
   c) Apply programming waveforms (step 17): MF cell is now programmed (MF = 1, SB = 0).
   d) Go back to step 7.
   e) Set CELL[9:0] to 0000000001 (steps 7 to 16).
   f) Apply programming waveforms (step 17): SB cell is now programmed (MF = SB = 1).
   g) Execute steps 18 to 20.
6. Programming waveforms MUST only be applied at step 17.

Table 16 Programming parameters

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{SDIN}	voltage applied to pin SDIN relative to V_{SS1}	notes 1 and 3				
		programming active	11	11.5	12	V
		programming inactive	0	–	V_{DD1}	V
V_{LCDIN}	voltage applied to pin V_{LCDIN} relative to V_{SS1}	notes 1 and 2				
		programming active	9	9.5	10	V
		programming inactive	0	–	V_{DD2}	V
I_{LCDIN}	current drawn by V_{LCDIN} during programming	when programming a single bit to one	–	850	1000	µA
I_{SDIN}	current drawn by V_{SDIN} during programming		–	100	200	µA
$T_{amb(prog)}$	ambient temperature during programming		0	25	40	°C
$t_{su;SCLK}$	set-up of internal data after last clock		1	–	–	µs
$t_{h;SCLK}$	hold of internal data before next clock		1	–	–	µs
$t_{su;SDIN}$	set-up of V_{SDIN} prior to programming		1	–	10	ms
$t_{h;SDIN}$	hold of V_{SDIN} after programming		1	–	10	ms
t_W	pulse width of programming voltage		100	120	200	ms

Notes

1. The voltage drop across the ITO track and zebra connector must be taken into account to guarantee sufficient voltage at the chip pins.
2. The high voltage generator must be disabled (V_{PR} = 0) when the V_{LCDIN} pin is being driven.
3. Maximum voltage must never be exceeded (even for a short time). Care must be taken when applying the programming waveforms in order to avoid overshoots.

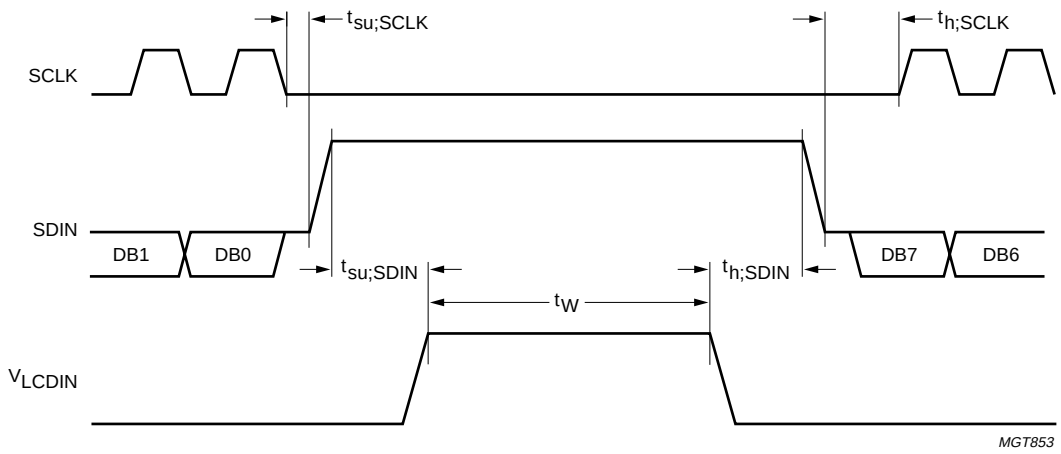


Fig.19 Programming waveforms.

20.7 Example of V_{LCD} calibration flow

The following tables are examples of the flow to calibrate V_{LCD}.

Table 17 V_{LCD} calibration flow 1

STEP	D/$\overline{C}$	COMMAND BYTE								ACTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1										switch power on
2										reset the device ($\overline{RES}$ pulse)
3										configure the device and fill in the DDRAM without switching the charge pump on
4	0	0	0	0	1	0	0	0	0	1	exit Power-down and set H = 1 instruction set
5										wait 5 ms
6	0	1	V_{PR6}	V_{PR5}	V_{PR4}	V_{PR3}	V_{PR2}	V_{PR1}	V_{PR0}	set V_{PR} and switch charge pump on
7										measure V_{LCD}
8	0	1	0	0	0	0	0	0	0	switch charge pump off
9										switch power off
10										calculate V_{CAL}[4:0] with look-up tables
11										store V_{CAL}[4:0] for programming later

Table 18 V_{LCD} calibration flow 2

STEP	D/$\overline{C}$	COMMAND BYTE								ACTION
		DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
1										switch power on
2										reset the device ($\overline{RES}$ pulse)
3										configure the device and fill in the DDRAM without switching the charge pump on
4	0	0	0	0	1	0	0	0	0	exit Power-down and set H = 0 instruction set
5										wait 5 ms
6	0	0	0	0	0	0	0	1	0	enter programming mode
7	0	1	0	0	0	0	0	0	CELL[9]	specify CELL[9] (V_{CAL}[4])
8	0	1	0	0	0	0	0	0	CELL[8]	specify CELL[8] (V_{CAL}[3])
9	0	1	0	0	0	0	0	0	CELL[7]	specify CELL[7] (V_{CAL}[2])
10	0	1	0	0	0	0	0	0	CELL[6]	specify CELL[6] (V_{CAL}[1])
11	0	1	0	0	0	0	0	0	CELL[5]	specify CELL[5] (V_{CAL}[0])
12	0	1	0	0	0	0	0	0	CELL[4]	specify CELL[4] (MF)
13	0	1	0	0	0	0	0	0	CELL[3]	specify CELL[3] (BS100)
14	0	1	0	0	0	0	0	0	CELL[2]	specify CELL[2] (TC1[1])
15	0	1	0	0	0	0	0	0	CELL[1]	specify CELL[1] (TC1[0])
16	0	0	0	0	0	0	0	0	1	specify CELL[0] = 1 (SB = 1)
17	0	0	0	1	0	0	0	0	1	set H = 1 instruction set (exit programming mode)
18	0	1	V_{PR6}	V_{PR5}	V_{PR4}	V_{PR3}	V_{PR2}	V_{PR1}	V_{PR0}	set V_{PR} and switch charge pump on
19										measure V_{LCD}
20	0	1	0	0	0	0	0	0	0	switch charge pump off
21										if V_{LCD} is not correct, go back to step 2 and try a different V_{CAL}[4:0]
22										switch power off
23										store V_{CAL}[4:0] for programming later

21 CHIP INFORMATION

The OM6213 is manufactured in n-well CMOS technology.

22 BONDING PAD INFORMATION

Table 19 Bonding pad information

NAME	ROW/COL SIDE	INTERFACE SIDE
Pad pitch	60 μm (min.)	70 μm (min.)
Pad size, aluminium	50 × 90 μm (min.)	60 × 100 μm (min.)
CBB opening	26 × 66 μm (min.)	36 × 76 μm (min.)
Bump dimensions	40 × 80 × 17.5 μm (±5) (min.)	50 × 90 × 17.5 μm (±5) (min.)
Wafer thickness (excluding bumps)	381 μm (±25)	

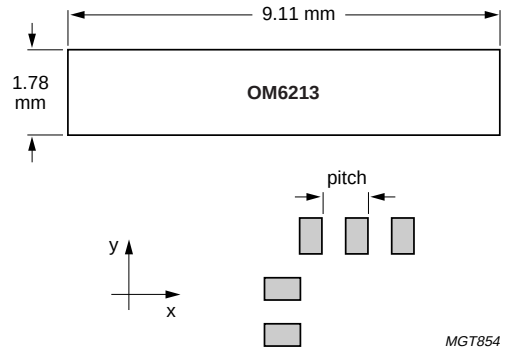


Fig.20 Bonding pads.

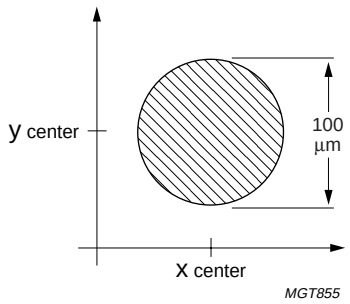


Fig.21 Shape of alignment mark (100 μm diameter).

23 BONDING PAD LOCATION

Table 20 Bonding pad location

All x and y co-ordinates are referenced to the centre of the chip (dimensions in μm; seeFig.22).

SYMBOL	PAD	COORDINATES	
		x	y
Dummy pad	1	–820	+4505
Alignment	2	–810	+4385
V_{OS4}	3	–820	+4240
V_{OS3}	4	–820	+4030
V_{OS2}	5	–820	+3680
V_{OS1}	6	–820	+3470
V_{OS0}	7	–820	+3120
Dummy pad	8	–820	+2700
Dummy pad	9	–820	+2420
Dummy pad	10	–820	+2350
Dummy pad	11	–820	+2280
Dummy pad	12	–820	+2210
V_{DD1}	13	–820	+2140
V_{DD1}	14	–820	+2070
V_{DD1}	15	–820	+2000
V_{DD1}	16	–820	+1930
V_{DD1}	17	–820	+1860
V_{DD1}	18	–820	+1790
V_{DD3}	19	–820	+1720
V_{DD3}	20	–820	+1650
V_{DD3}	21	–820	+1580
V_{DD3}	22	–820	+1510
V_{DD2}	23	–820	+1440
V_{DD2}	24	–820	+1370
V_{DD2}	25	–820	+1300
V_{DD2}	26	–820	+1230
V_{DD2}	27	–820	+1160
V_{DD2}	28	–820	+1090
V_{DD2}	29	–820	+1020
V_{DD2}	30	–820	+950
SCLK	31	–820	+880
T7	32	–820	+670
T7	33	–820	+600
T7	34	–820	+530
T7	35	–820	+460
SDIN	36	–820	+390
SDIN	37	–820	+320
SDIN	38	–820	+250
SDIN	39	–820	+180
D/$\overline{C}$	40	–820	+110
$\overline{SCE}$	41	–820	–100
OSC	42	–820	–310
V_{SS2}	43	–820	–520
V_{SS2}	44	–820	–590
V_{SS2}	45	–820	–660
V_{SS2}	46	–820	–730
V_{SS2}	47	–820	–800
V_{SS2}	48	–820	–870
V_{SS2}	49	–820	–940
V_{SS2}	50	–820	–1010
T4	51	–820	–1080
T5	52	–820	–1290
T6	53	–820	–1500
V_{SS1}	54	–820	–1710
V_{SS1}	55	–820	–1780
V_{SS1}	56	–820	–1850
V_{SS1}	57	–820	–1920
V_{SS1}	58	–820	–1990
V_{SS1}	59	–820	–2060
V_{SS1}	60	–820	–2130
V_{SS1}	61	–820	–2200
T1	62	–820	–2410
T2	63	–820	–2620
T3	64	–820	–2830
V_{LCDIN}	65	–820	–3180
V_{LCDIN}	66	–820	–3250
V_{LCDIN}	67	–820	–3320
V_{LCDIN}	68	–820	–3390
V_{LCDIN}	69	–820	–3460
V_{LCDIN}	70	–820	–3530
V_{LCDOUT}	71	–820	–3600
V_{LCDOUT}	72	–820	–3670
V_{LCDOUT}	73	–820	–3740
V_{LCDOUT}	74	–820	–3810
V_{LCDOUT}	75	–820	–3880

SYMBOL	PAD	COORDINATES	
		x	y
V_{LCDOUT}	76	–820	–3950
V_{LCDOUT}	77	–820	–4020
VLCDSEN	78	–820	–4090
$\overline{RES}$	79	–820	–4160
Alignment	80	–810	–4400
Dummy pad	81	–820	–4505
Dummy pad	82	+825	–4495
Dummy pad	83	+825	–4435
Dummy pad	84	+825	–4375
Dummy pad	85	+825	–4315
Dummy pad	86	+825	–4255
Dummy pad	87	+825	–4195
Dummy pad	88	+825	–4135
ROW 11	89	+825	–3955
ROW 10	90	+825	–3895
ROW 9	91	+825	–3835
ROW 8	92	+825	–3775
ROW 7	93	+825	–3715
ROW 6	94	+825	–3655
ROW 5	95	+825	–3595
ROW 4	96	+825	–3535
ROW 3	97	+825	–3475
ROW 2	98	+825	–3415
ROW 1	99	+825	–3355
ROW 0	100	+825	–3295
ROW 12	101	+825	–3235
ROW 13	102	+825	–3175
ROW 14	103	+825	–3115
ROW 15	104	+825	–3055
ROW 16	105	+825	–2995
ROW 17	106	+825	–2935
ROW 18	107	+825	–2875
ROW 19	108	+825	–2815
ROW 20	109	+825	–2755
ROW 21	110	+825	–2695
ROW 22	111	+825	–2635
ROW 23	112	+825	–2575
COL 0	113	+825	–2395
COL 1	114	+825	–2335

SYMBOL	PAD	COORDINATES	
		x	y
COL 2	115	+825	–2275
COL 3	116	+825	–2215
COL 4	117	+825	–2155
COL 5	118	+825	–2095
COL 6	119	+825	–2035
COL 7	120	+825	–1975
COL 8	121	+825	–1915
COL 9	122	+825	–1855
COL 10	123	+825	–1795
COL 11	124	+825	–1735
COL 12	125	+825	–1675
COL 13	126	+825	–1615
COL 14	127	+825	–1555
COL 15	128	+825	–1495
COL 16	129	+825	–1435
COL 17	130	+825	–1375
COL 18	131	+825	–1315
COL 19	132	+825	–1255
COL 20	133	+825	–1195
COL 21	134	+825	–1135
COL 22	135	+825	–1075
COL 23	136	+825	–1015
COL 24	137	+825	–955
COL 25	138	+825	–895
COL 26	139	+825	–835
COL 27	140	+825	–775
COL 28	141	+825	–595
COL 29	142	+825	–535
COL 30	143	+825	–475
COL 31	144	+825	–415
COL 32	145	+825	–355
COL 33	146	+825	–295
COL 34	147	+825	–235
COL 35	148	+825	–175
COL 36	149	+825	–115
COL 37	150	+825	–55
COL 38	151	+825	+5
COL 39	152	+825	+65
COL 40	153	+825	+125

SYMBOL	PAD	COORDINATES	
		x	y
COL 41	154	+825	+185
COL 42	155	+825	+245
COL 43	156	+825	+305
COL 44	157	+825	+365
COL 45	158	+825	+425
COL 46	159	+825	+485
COL 47	160	+825	+545
COL 48	161	+825	+605
COL 49	162	+825	+665
COL 50	163	+825	+725
COL 51	164	+825	+785
COL 52	165	+825	+845
COL 53	166	+825	+905
COL 54	167	+825	+965
COL 55	168	+825	+1025
COL 56	169	+825	+1205
COL 57	170	+825	+1265
COL 58	171	+825	+1325
COL 59	172	+825	+1385
COL 60	173	+825	+1445
COL 61	174	+825	+1505
COL 62	175	+825	+1565
COL 63	176	+825	+1625
COL 64	177	+825	+1685
COL 65	178	+825	+1745
COL 66	179	+825	+1805
COL 67	180	+825	+1865
COL 68	181	+825	+1925
COL 69	182	+825	+1985
COL 70	183	+825	+2045
COL 71	184	+825	+2105
COL 72	185	+825	+2165
COL 73	186	+825	+2225
COL 74	187	+825	+2285
COL 75	188	+825	+2345

SYMBOL	PAD	COORDINATES	
		x	y
COL 76	189	+825	+2405
COL 77	190	+825	+2465
COL 78	191	+825	+2525
COL 79	192	+825	+2585
COL 80	193	+825	+2645
COL 81	194	+825	+2705
COL 82	195	+825	+2765
COL 83	196	+825	+2825
ROW 47	197	+825	+3005
ROW 46	198	+825	+3065
ROW 45	199	+825	+3125
ROW 44	200	+825	+3185
ROW 43	201	+825	+3245
ROW 42	202	+825	+3305
ROW 41	203	+825	+3365
ROW 40	204	+825	+3425
ROW 39	205	+825	+3485
ROW 38	206	+825	+3545
ROW 37	207	+825	+3605
ROW 36	208	+825	+3665
ROW 24	209	+825	+3725
ROW 25	210	+825	+3785
ROW 26	211	+825	+3845
ROW 27	212	+825	+3905
ROW 28	213	+825	+3965
ROW 29	214	+825	+4025
ROW 30	215	+825	+4085
ROW 31	216	+825	+4145
ROW 32	217	+825	+4205
ROW 33	218	+825	+4265
ROW 34	219	+825	+4325
ROW 35	220	+825	+4385
Dummy pad	221	+825	+4445
Dummy pad	222	+825	+4505

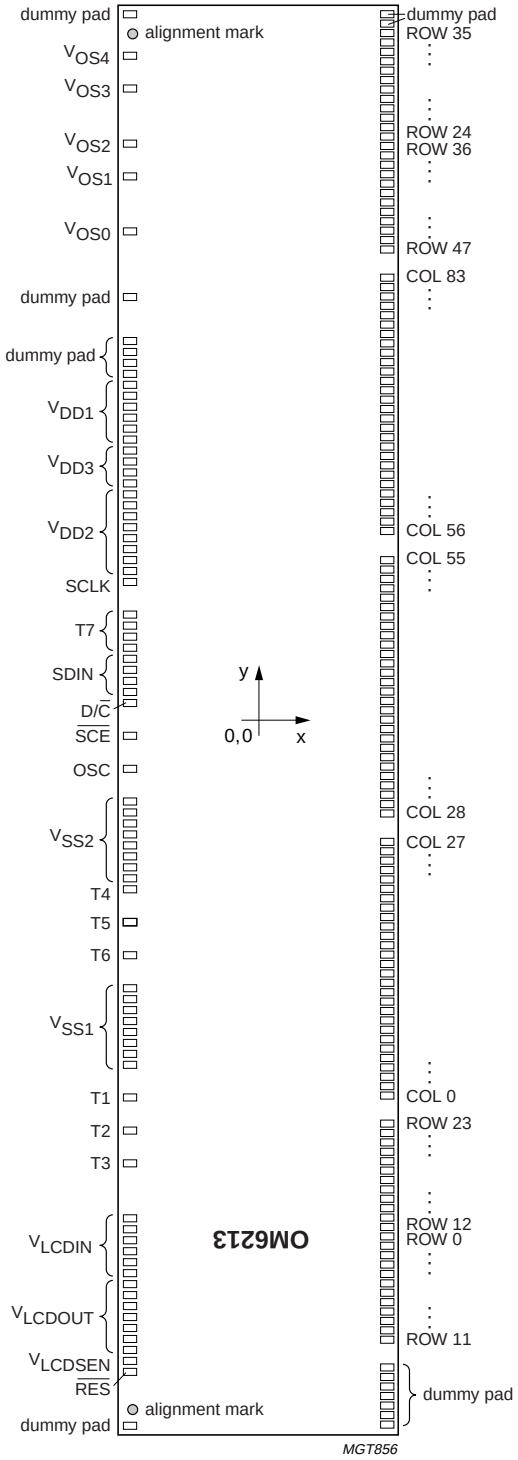
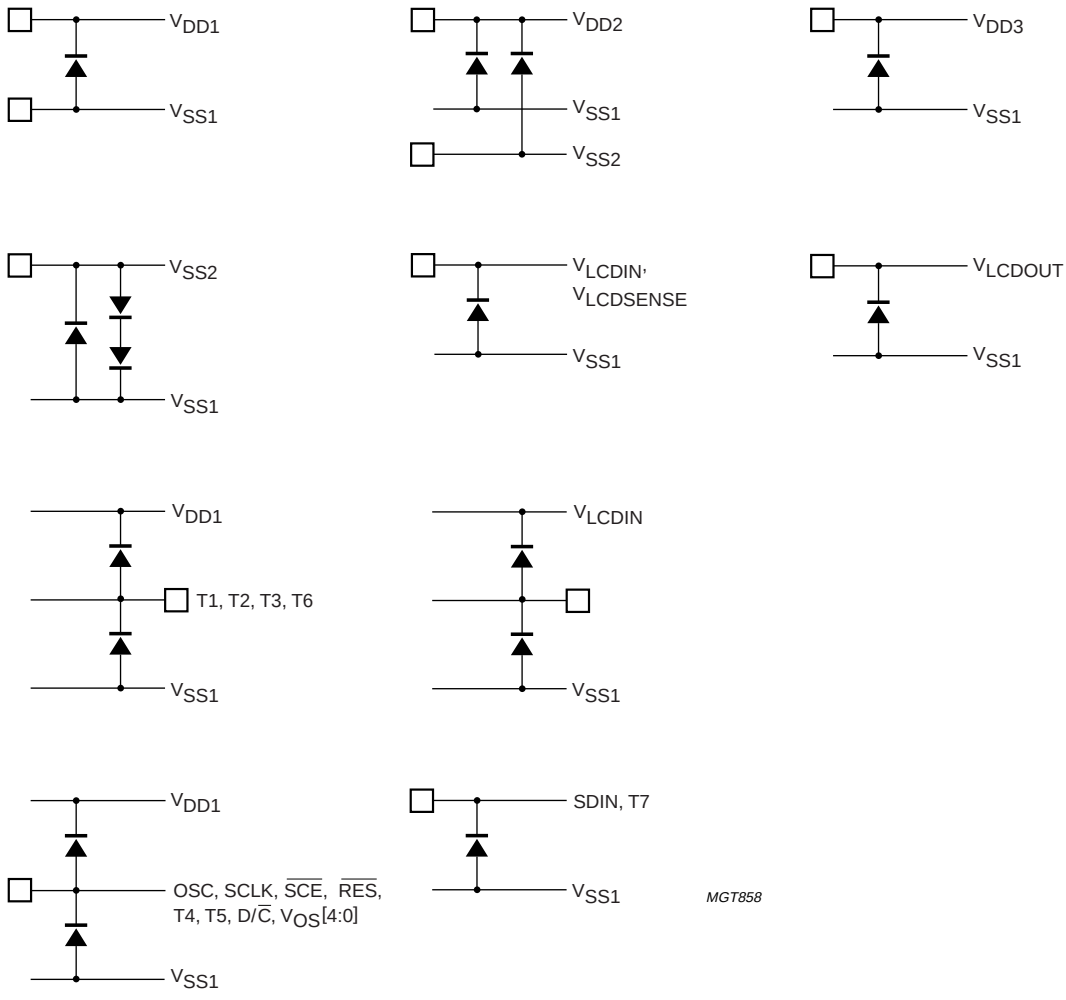


Fig.22 Pad locations.

24 DEVICE PROTECTION DIAGRAM



The conditions for continuity test are as follows:
Maximum forward current = 5 mA; Maximum reverse voltage = 5 V.

Fig.23 Device protection diagram.

25 TRAY INFORMATION

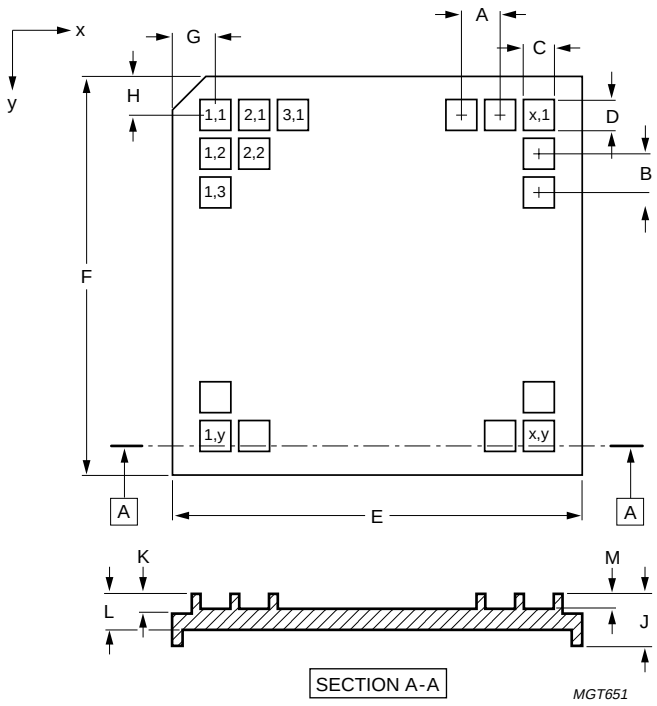
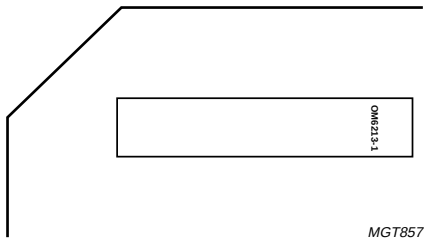


Fig.24 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram for the orientating and position of the type name on the surface.

Fig.25 Tray alignment.

Table 21 Tray dimensions

DIMENSION	DESCRIPTION	VALUE
A	pocket pitch, x direction	14.45 mm
B	pocket pitch, y direction	3.76 mm
C	pocket width, x direction	9.31 mm
D	pocket width, y direction	1.98 mm
E	tray width, x direction	50.8 mm
F	tray width, y direction	50.8 mm
G	distance from cut corner to pocket (1 and 1) centre	10.95 mm
H	distance from cut corner to pocket (1 and 1) centre	4.72 mm
J	tray thickness	3.96 mm
K	tray cross section	1.78 mm
L	tray cross section	2.44 mm
M	pocket depth	0.89 mm
x	number of pockets in x direction	3
y	number of pockets in y direction	12

26 DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
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